CEM831 Series

Intel® Atom™
COM Express Type-II Module

User's Manual

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CAUTION

If you replace wrong batteries, it causes the danger of explosion. It is recommended by the manufacturer that you follow the manufacturer's instructions to only replace the same or equivalent type of battery, and dispose of used ones.

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ESD Precautions

Computer boards have integrated circuits sensitive to static electricity. To prevent chipsets from electrostatic discharge damage, please take care of the following jobs with precautions:

- Do not remove boards or integrated circuits from their anti-static packaging until you are ready to install them.
- Before holding the board or integrated circuit, touch an unpainted portion of the system unit chassis for a few seconds. It discharges static electricity from your body.
- Wear a wrist-grounding strap, available from most electronic component stores, when handling boards and components.

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Chapter 1

Introduction

The **CEM831** is a new COM Express™ Type-II Module to support Intel® N270 with 533MHz FSB and integrates Intel® 945GME & ICH7M chipsets.

This powerful module supports excellent Multiple I/O, LVDS LCD, Gigabit Ethernet, HD digital Audio, one PATA -100, two SATA and eight USB 2.0 ports to make all in one single module as computing engine. It provides one PCI Express x16 for graphics or SDVO, three PCI Express X1, and four 32-bit/33MHz PCI master for expansion purpose.

It can achieve the best stability and reliability that makes your system perform the most endurable operation in any critical environments. The built-in Watchdog Timer has enhanced the system reliability that achieves a unique feature to distinguish itself from other boards.

1.1 Specifications

CPU: Intel® Atom™ N270 1.6GHz/512KB L2 cache processor

- **CPU Frequency: FSB533MHz**
- **System Chipset:** Intel® 945GME and ICH7M

  Intel® 945GME and ICH7M – DH (Option)
- **BIOS**
  - AMI BIOS
  - 8 Mbit SPI Flash, DMI, Plug and Play
  - RPL/PXE Ethernet Boot ROM
  - SmartView for multiple LCD type selection, display mode option and application extension features
  - "Load Optimized Default" customized Setting in the BIOS flash chip to prevent from CMOS battery fail
  - LPC-free supported.
- **System Memory**
  - Two x 200-pin DDR2 SO-DIMM sockets
  - Maximum to 4GB DDR2 SDRAMs. (Intel 945GME supports DDR2-400/533 up to 4GB; the actual maximum capacity will be less depending on system configuration)
- **IDE**
  - One PATA port supported through COM Express connector.
  - Two SATA-150 ports supported through COM Express connector.
- **USB Interface**
  - Eight USB ports complies with USB Spec. Rev. 2.0

- **Graphics:**
  - Intel® 945GME GMCH Gen 3.5 integrated graphic engine
  - CRT and LVDS LCD output
  - Maximum up to 224MB frame buffer sharing system memory
  - Maximum display resolution:
    - CRT: 2048 X 1536
    - LVDS: 1366 X 768 (18 or 24-bit),
      1920 X 1200 (36-bit)
      1920 X 1080 (48-bit)

- **Expansion Interface:**
  - One PCI Express x16 interface for SDVO ADD2+ Card as default (PCI Express x16 for discrete graphics is optional with on-board LVDS function removal)
  - Three PCI Express x1 interfaces
  - Four 32-bit/33MHz PCI masters
- **Ethernet:**
  - Intel 82583V for PCI-E Gigabit Ethernet and optional with co-layout as Intel 82574L for Gigabit Ethernet.
- **Audio:**
  - HD Audio
- **Power Management:**
  - ACPI (Advanced Configuration and Power Interface)

***NOTE**: All specifications and images are subject to change without notice.*

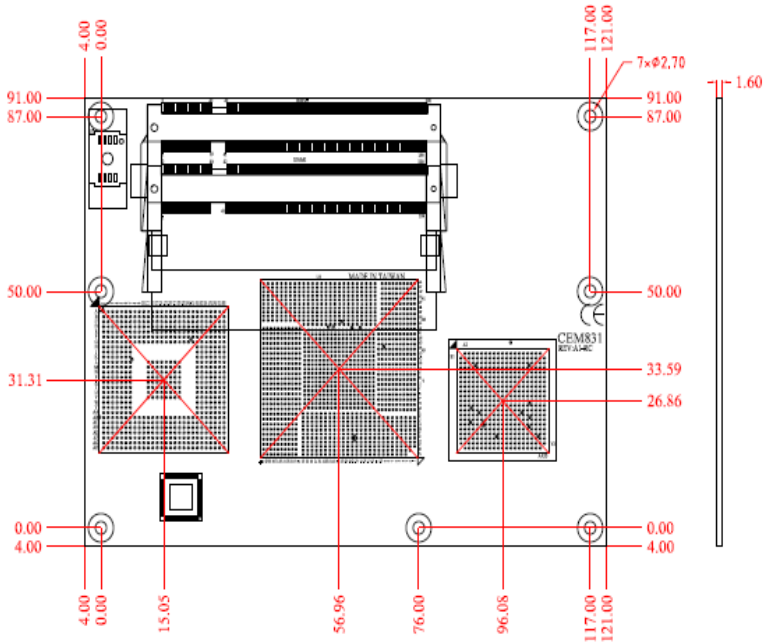
1.2 Utilities Supported

- Chipset Driver
- VGA Driver
- Ethernet Driver
- Audio Driver

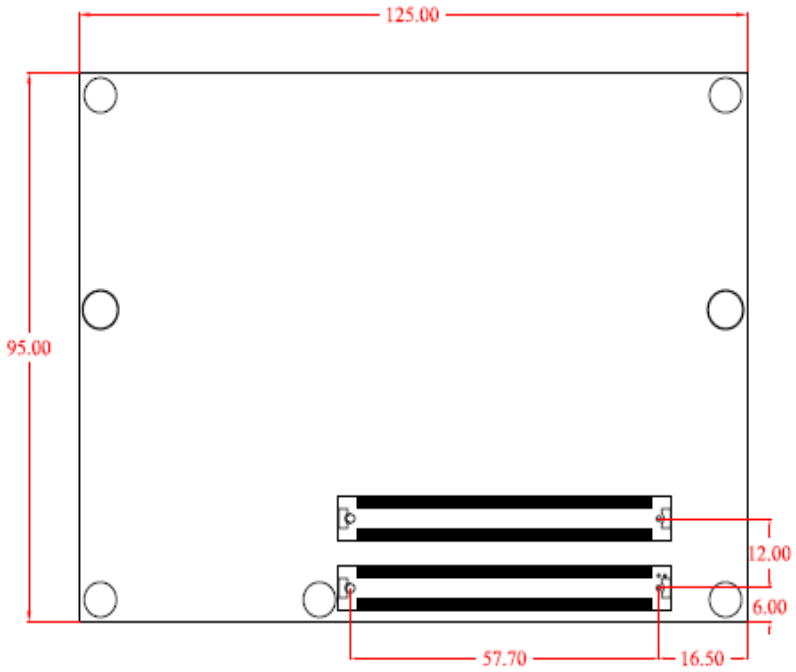
Chapter 2

Board Layout and Pin Assignments

2.1 Board Dimensions and Fixing Holes

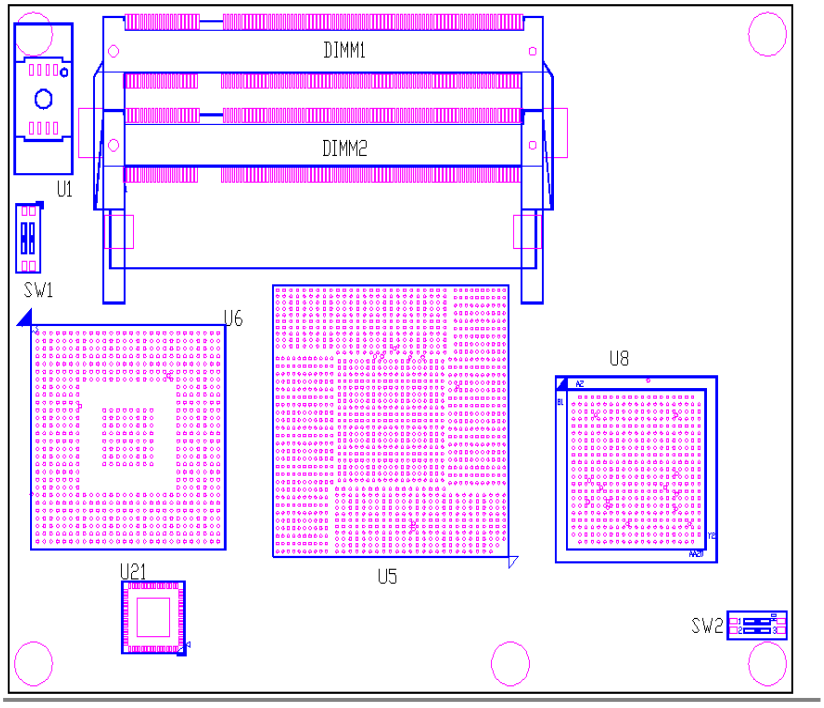


Component Side

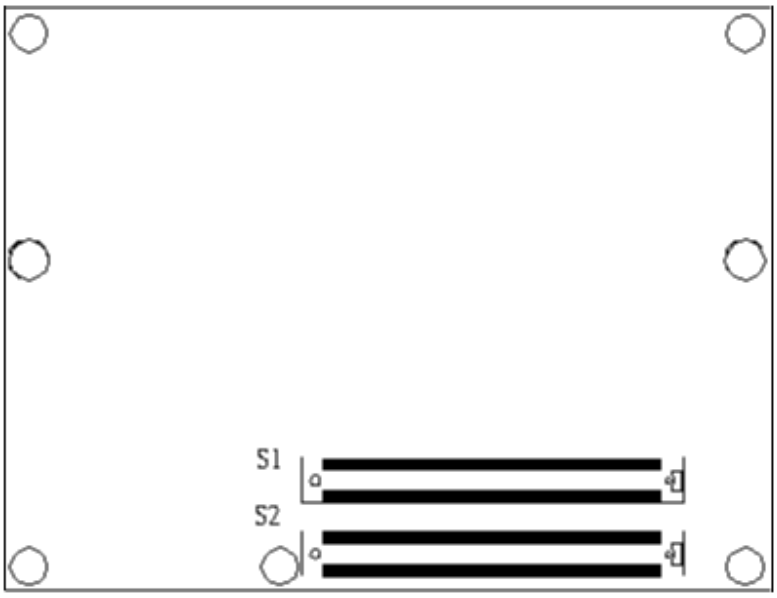


Solder Side

2.2 Board Layout



Component Side



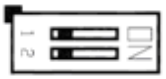
Solder Side

2.3 Jumper Settings

1. PCI-Express X1 or X4 Select (SW1)

Description	Settings	SW1
PCI-E x1 (Port 1-4)	OFF (Default)	
PCI-E x4	ON	

2. AT or ATX Select (SW2)

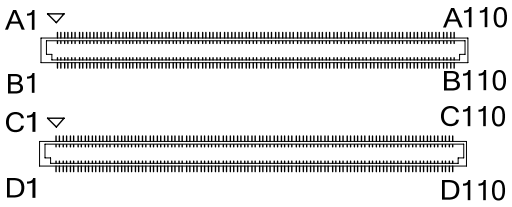
Description	Settings	SW2
ATX	OFF (Default)	
AT	ON	

2.4 Connectors

The connectors allow the CPU Board to connect with other parts of the system. Some problems encountered by your system may be a result from loose or improper connections. Ensure that all connectors are in place and firmly attached. The following table lists the function of each connector on the CEM831.

Connectors	Label
DDRII SODIMM Connector	DIMM1
DDRII SODIMM Connector	DIMM2
COM Express™ Connector	S1
COM Express™ Connector	S2

S1, S2：COM Express™ Connector



Pin	Description	Pin	Description	Pin	Description	Pin	Description
A1	GND (FIXED)	B1	GND (FIXED)	C1	GND (FIXED)	D1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#	C2	IDE_D7	D2	IDE_D5
A3	GBE0_MDI3+	B3	LPC_FRAME#	C3	IDE_D6	D3	IDE_D10
A4	GBE0_LINK100#	B4	LPC_AD0	C4	IDE_D3	D4	IDE_D11
A5	GBE0_LINK1000#	B5	LPC_AD1	C5	IDE_D15	D5	IDE_D12
A6	GBE0_MDI2-	B6	LPC_AD2	C6	IDE_D8	D6	IDE_D4
A7	GBE0_MDI2+	B7	LPC_AD3	C7	IDE_D9	D7	IDE_D0
A8	GBE0_LINK#	B8	LPC_DRQ0#	C8	IDE_D2	D8	IDE_REQ
A9	GBE0_MDI1-	B9	LPC_DRQ1#	C9	IDE_D13	D9	IDE_IOW#
A10	GBE0_MDI1+	B10	LPC_CLK	C10	IDE_D1	D10	IDE_ACK#
A11	GND (FIXED)	B11	GND (FIXED)	C11	GND (FIXED)	D11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#	C12	IDE_D14	D12	IDE_IRQ
A13	GBE0_MDI0+	B13	SMB_CK	C13	IDE_IORDY	D13	IDE_A0
A14	GBE0_CTREF	B14	SMB_DAT	C14	IDE_IOR#	D14	IDE_A1
A15	SUS_S3#	B15	SMB_ALERT#	C15	PCI_PME#	D15	IDE_A2
A16	SATA0_TX+	B16	SATA1_TX+	C16	PCI_GNT2#	D16	IDE_CS1#
A17	SATA0_TX-	B17	SATA1_TX-	C17	PCI_REQ2#	D17	IDE_CS3#
A18	SUS_S4#	B18	SUS_STAT#	C18	PCI_GNT1#	D18	IDE_RESET#
A19	SATA0_RX+	B19	SATA1_RX+	C19	PCI_REQ1#	D19	PCI_GNT3#
A20	SATA0_RX-	B20	SATA1_RX-	C20	PCI_GNT0#	D20	PCI_REQ3#
A21	GND (FIXED)	B21	GND (FIXED)	C21	GND (FIXED)	D21	GND (FIXED)
A22	N.C	B22	N.C	C22	PCI_REQ0#	D22	PCI_AD1
A23	N.C	B23	N.C	C23	PCI_RESET#	D23	PCI_AD3
A24	SUS_S5#	B24	PWR_OK	C24	PCI_AD0	D24	PCI_AD5
A25	N.C	B25	N.C	C25	PCI_AD2	D25	PCI_AD7
A26	N.C	B26	N.C	C26	PCI_AD4	D26	PCI_C/BE0#
A27	BATLOW#	B27	WDT	C27	PCI_AD6	D27	PCI_AD9
A28	ATA_ACT#	B28	AC_SDIN2	C28	PCI_AD8	D28	PCI_AD11
A29	AC_SYNC	B29	AC_SDIN1	C29	PCI_AD10	D29	PCI_AD13
A30	AC_RST#	B30	AC_SDIN0	C30	PCI_AD12	D30	PCI_AD15
A31	GND (FIXED)	B31	GND (FIXED)	C31	GND (FIXED)	D31	GND (FIXED)
A32	AC_BITCLK	B32	SPKR	C32	PCI_AD14	D32	PCI_PAR
A33	AC_SDOUT	B33	I2C_CK	C33	PCI_C/BE1#	D33	PCI_SERR#
A34	N.C	B34	I2C_DAT	C34	PCI_PERR#	D34	PCI_STOP#

Pin	Description	Pin	Description	Pin	Description	Pin	Description
A35	THRMTRIP#	B35	THRM#	C35	PCI_LOCK#	D35	PCI_TRDY#
A36	USB6-	B36	USB7-	C36	PCI_DEVSEL#	D36	PCI_FRAME#
A37	USB6+	B37	USB7+	C37	PCI_IRDY#	D37	PCI_AD16
A38	USB_6_7_OC#	B38	USB_4_5_OC#	C38	PCI_C/BE2#	D38	PCI_AD18
A39	USB4-	B39	USB5-	C39	PCI_AD17	D39	PCI_AD20
A40	USB4+	B40	USB5+	C40	PCI_AD19	D40	PCI_AD22
A41	GND (FIXED)	B41	GND (FIXED)	C41	GND (FIXED)	D41	GND (FIXED)
A42	USB2-	B42	USB3-	C42	PCI_AD21	D42	PCI_AD24
A43	USB2+	B43	USB3+	C43	PCI_AD23	D43	PCI_AD26
A44	USB_2_3_OC#	B44	USB_0_1_OC#	C44	PCI_C/BE3#	D44	PCI_AD28
A45	USB0-	B45	USB1-	C45	PCI_AD25	D45	PCI_AD30
A46	USB0+	B46	USB1+	C46	PCI_AD27	D46	PCI_IRQC#
A47	VCC_RTC	B47	EXCD1_PERST#	C47	PCI_AD29	D47	PCI_IRQD#
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	C48	PCI_AD31	D48	PCI_CLKRUN#
A49	EXCD0_CPPE#	B49	SYS_RESET#	C49	PCI_IRQA#	D49	N.C
A50	LPC_SERIRQ	B50	CB_RESET#	C50	PCI_IRQB#	D50	PCI_CLK
A51	GND (FIXED)	B51	GND (FIXED)	C51	GND (FIXED)	D51	GND (FIXED)
A52	*PCIE_TX0+	B52	*PCIE_RX0+	C52	PEG_RX0+	D52	PEG_TX0+
A53	*PCIE_TX0-	B53	*PCIE_RX0-	C53	PEG_RX0-	D53	PEG_TX0-
A54	GPI0	B54	GPO1	C54	N.C	D54	PEG_LANE_RV#
A55	N.C	B55	N.C	C55	PEG_RX1+	D55	PEG_TX1+
A56	N.C	B56	N.C	C56	PEG_RX1-	D56	PEG_TX1-
A57	GND	B57	GPO2	C57	N.C	D57	N.C
A58	N.C	B58	N.C	C58	PEG_RX2+	D58	PEG_TX2+
A59	N.C	B59	N.C	C59	PEG_RX2-	D59	PEG_TX2-
A60	GND (FIXED)	B60	GND (FIXED)	C60	GND (FIXED)	D60	GND (FIXED)
A61	PCIE_TX3+	B61	PCIE_RX3+	C61	PEG_RX3+	D61	PEG_TX3+
A62	PCIE_TX3-	B62	PCIE_RX3-	C62	PEG_RX3-	D62	PEG_TX3-
A63	GPI1	B63	GPO3	C63	RSVD	D63	RSVD
A64	PCIE_TX2+	B64	PCIE_RX2+	C64	RSVD	D64	RSVD
A65	PCIE_TX2-	B65	PCIE_RX2-	C65	PEG_RX4+	D65	PEG_TX4+
A66	GND	B66	WAKE0#	C66	PEG_RE4-	D66	PEG_TX4-
A67	GPI2	B67	WAKE1#	C67	RSVD	D67	GND
A68	PCIE_TX1+	B68	PCIE_RX1+	C68	PEG_RX5+	D68	PEG_TX5+
A69	PCIE_TX1-	B69	PCIE_RX1-	C69	PEG_RX5-	D69	PEG_TX5-

A70	GND(FIXED)	B70	GND(FIXED)	C70	GND(FIXED)	D70	GND(FIXED)
Pin	**Description**	**Pin**	**Description**	**Pin**	**Description**	**Pin**	**Description**
A71	LVDS_A0+	B71	LVDS_B0+	C71	PEG_RX6+	D71	PEG_TX6+
A72	LVDS_A0-	B72	LVDS_B0-	C72	PEG_RX6-	D72	PEG_TX6-
A73	LVDS_A1+	B73	LVDS_B1+	C73	SDVO_DATA	D73	SDVO_CLK
A74	LVDS_A1-	B74	LVDS_B1-	C74	PEG_RX7+	D74	PEG_TX7+
A75	LVDS_A2+	B75	LVDS_B2+	C75	PEG_RX7-	D75	PEG_TX7-
A76	LVDS_A2-	B76	LVDS_B2-	C76	GND	D76	GND
A77	LVDS_VDD_EN	B77	**LVDS_B3+	C77	RSVD	D77	IDE_CBLID#
A78	**LVDS_A3+	B78	**LVDS_B3-	C78	PEG_RX8+	D78	PEG_TX8+
A79	**LVDS_A3-	B79	LVDS_BKLT_EN	C79	PEG_RX8-	D79	PEG_TX8-
A80	GND(FIXED)	B80	GND(FIXED)	C80	GND(FIXED)	D80	GND(FIXED)
A81	LVDS_A_CK+	B81	LVDS_B_CK+	C81	PEG_RX9+	D81	PEG_TX9+
A82	LVDS_A_CK-	B82	LVDS_B_CK-	C82	PEG_RX9-	D82	PEG_TX9-
A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL	C83	RSVD	D83	RSVD
A84	LVDS_I2C_DAT	B84	VCC_5V_SBY	C84	GND	D84	GND
A85	GPI3	B85	VCC_5V_SBY	C85	PEG_RX10+	D85	PEG_TX10+
A86	KBD_RST#	B86	VCC_5V_SBY	C86	PEG_RX10-	D86	PEG_TX10-
A87	KBD_A20GATE	B87	VCC_5V_SBY	C87	GND	D87	GND
A88	PCIE0_CK_REF+	B88	RSVD	C88	PEG_RX11+	D88	PEG_TX11+
A89	PCIE0_CK_REF-	B89	VGA_RED	C89	PEG_RX11-	D89	PEG_TX11-
A90	GND (FIXED)	B90	GND (FIXED)	C90	GND (FIXED)	D90	GND (FIXED)
A91	RSVD	B91	VGA_GRN	C91	PEG_RX12+	D91	PEG_TX12+
A92	RSVD	B92	VGA_BLU	C92	PEG_RX12-	D92	PEG_TX12-
A93	GPO0	B93	VGA_HSYNC	C93	GND	D93	GND
A94	RSVD	B94	VGA_VSYNC	C94	PEG_RX13+	D94	PEG_TX13+
A95	RSVD	B95	VGA_I2C_CK	C95	PEG_RX13-	D95	PEG_TX13-
A96	GND	B96	VGA_I2C_DAT	C96	GND	D96	GND

Pin	Description	Pin	Description	Pin	Description	Pin	Description
A97	VCC_12V	B97	TV_DAC_A	C97	RSVD	D97	N.C
A98	VCC_12V	B98	TV_DAC_B	C98	PEG_RX14+	D98	PEG_TX14+
A99	VCC_12V	B99	TV_DAC_C	C99	PEG_RX14-	D99	PEG_TX14-
A100	GND (FIXED)	B100	GND (FIXED)	C100	GND (FIXED)	D100	GND (FIXED)
A101	VCC_12V	B101	VCC_12V	C101	PEG_RX15+	D101	PEG_TX15+
A102	VCC_12V	B102	VCC_12V	C102	PEG_RX15-	D102	PEG_TX15-
A103	VCC_12V	B103	VCC_12V	C103	GND	D103	GND
A104	VCC_12V	B104	VCC_12V	C104	VCC_12V	D104	VCC_12V
A105	VCC_12V	B105	VCC_12V	C105	VCC_12V	D105	VCC_12V
A106	VCC_12V	B106	VCC_12V	C106	VCC_12V	D106	VCC_12V
A107	VCC_12V	B107	VCC_12V	C107	VCC_12V	D107	VCC_12V
A108	VCC_12V	B108	VCC_12V	C108	VCC_12V	D108	VCC_12V
A109	VCC_12V	B109	VCC_12V	C109	VCC_12V	D109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)	C110	GND (FIXED)	D110	GND (FIXED)

-- End of COM Express™ Table --

Chapter 3
Hardware Description

3.1 Microprocessors

The CEM831 Series supports Intel® Atom™ processor N270, which make your system operated under Windows XP, Windows Vista, Windows 7 and Linux environments. The system performance depends on the microprocessor. Make sure your installed microprocessor with all correct settings that prevent the CPU from damages.

3.2 BIOS

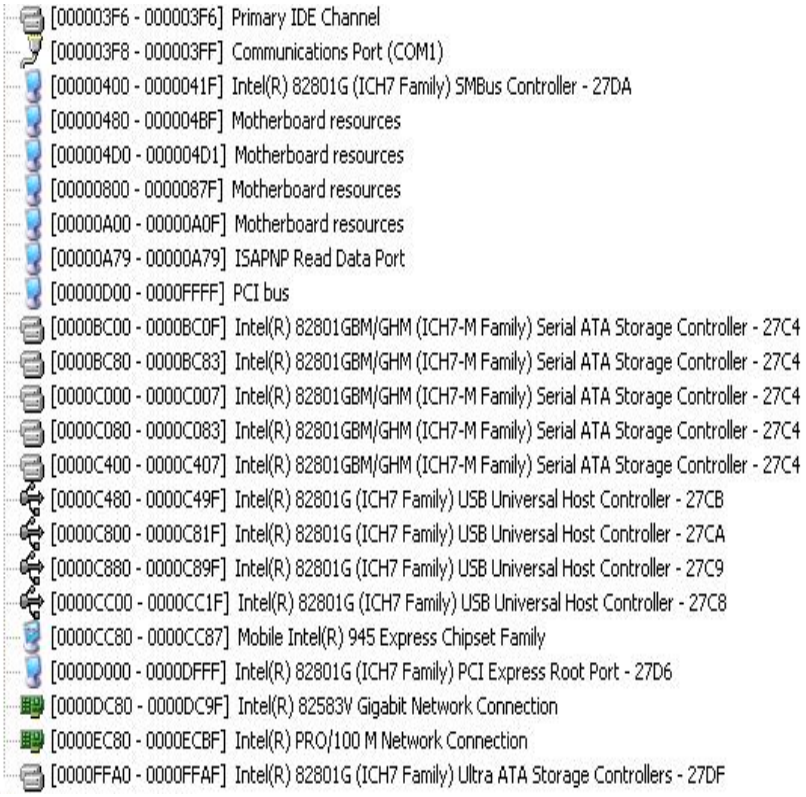
The CEM831 Series uses AMI Plug and Play BIOS with a single 8Mbit SPI Flash, DMI, Plug and Play.

3.3 System Memory

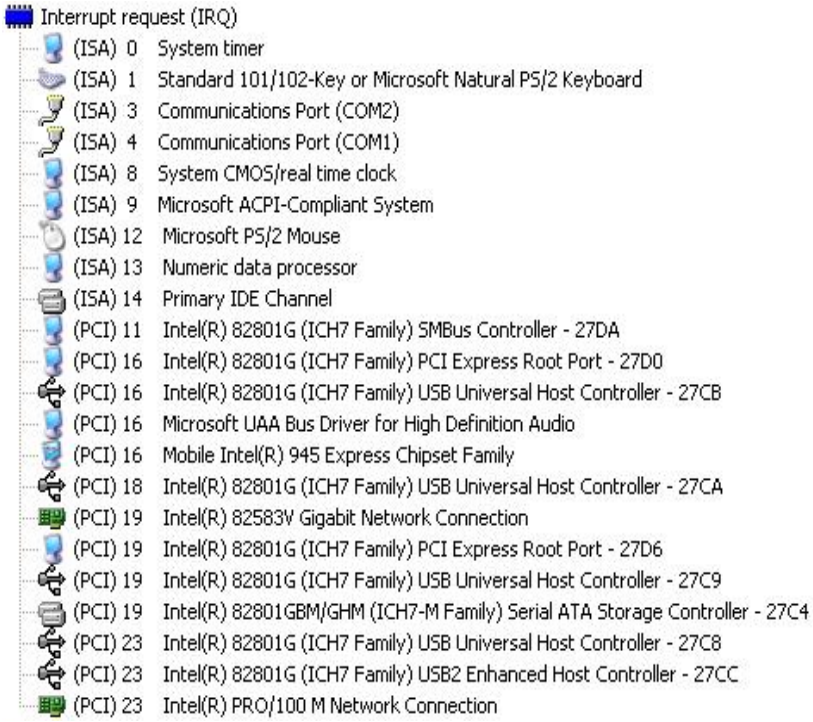
The CEM831 Series industrial CPU card supports two 200-pin DDR2 SO-DIMM sockets for a maximum memory of 4GB DDR2 SDRAMs. (Intel 945GME supports DDR2-400/533 up to 4GB; the actual maximum capacity will be less depending on system configuration) The memory module can come in sizes of 256MB, 512MB, 1GB and 2GB.

3.4 I/O Port Address Map (With CEB94000 under WinXP)

Input/output (IO)
[00000000 - 0000000F] Direct memory access controller
[00000000 - 00000CF7] PCI bus
[00000010 - 0000001F] Motherboard resources
[00000020 - 00000021] Programmable interrupt controller
[00000022 - 0000003F] Motherboard resources
[00000040 - 00000043] System timer
[00000044 - 0000005F] Motherboard resources
[00000060 - 00000060] Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
[00000061 - 00000061] System speaker
[00000063 - 00000063] Motherboard resources
[00000064 - 00000064] Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
[00000065 - 00000065] Motherboard resources
[00000067 - 0000006F] Motherboard resources
[00000070 - 00000071] System CMOS/real time clock
[00000072 - 0000007F] Motherboard resources
[00000080 - 00000080] Motherboard resources
[00000081 - 00000083] Direct memory access controller
[00000084 - 00000086] Motherboard resources
[00000087 - 00000087] Direct memory access controller
[00000088 - 00000088] Motherboard resources
[00000089 - 0000008B] Direct memory access controller
[0000008C - 0000008E] Motherboard resources
[0000008F - 0000008F] Direct memory access controller
[00000090 - 0000009F] Motherboard resources
[000000A0 - 000000A1] Programmable interrupt controller
[000000A2 - 000000BF] Motherboard resources
[000000C0 - 000000DF] Direct memory access controller
[000000E0 - 000000EF] Motherboard resources
[000000F0 - 000000FF] Numeric data processor
[000001F0 - 000001F7] Primary IDE Channel
[00000274 - 00000277] ISAPNP Read Data Port
[00000279 - 00000279] ISAPNP Read Data Port
[000002F8 - 000002FF] Communications Port (COM2)
[00000378 - 0000037F] Printer Port (LPT1)
[000003B0 - 000003BB] Mobile Intel(R) 945 Express Chipset Family
[000003C0 - 000003DF] Mobile Intel(R) 945 Express Chipset Family


[000003F6 - 000003F6] Primary IDE Channel
[000003F8 - 000003FF] Communications Port (COM1)
[00000400 - 0000041F] Intel(R) 82801G (ICH7 Family) SMBus Controller - 27DA
[00000480 - 000004BF] Motherboard resources
[000004D0 - 000004D1] Motherboard resources
[00000800 - 0000087F] Motherboard resources
[00000A00 - 00000A0F] Motherboard resources
[00000A79 - 00000A79] ISAPNP Read Data Port
[00000D00 - 0000FFFF] PCI bus
[0000BC00 - 0000BC0F] Intel(R) 82801GBM/GHM (ICH7-M Family) Serial ATA Storage Controller - 27C4
[0000BC80 - 0000BC83] Intel(R) 82801GBM/GHM (ICH7-M Family) Serial ATA Storage Controller - 27C4
[0000C000 - 0000C007] Intel(R) 82801GBM/GHM (ICH7-M Family) Serial ATA Storage Controller - 27C4
[0000C080 - 0000C083] Intel(R) 82801GBM/GHM (ICH7-M Family) Serial ATA Storage Controller - 27C4
[0000C400 - 0000C407] Intel(R) 82801GBM/GHM (ICH7-M Family) Serial ATA Storage Controller - 27C4
[0000C480 - 0000C49F] Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27CB
[0000C800 - 0000C81F] Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27CA
[0000C880 - 0000C89F] Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27C9
[0000CC00 - 0000CC1F] Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27C8
[0000CC80 - 0000CC87] Mobile Intel(R) 945 Express Chipset Family
[0000D000 - 0000DFFF] Intel(R) 82801G (ICH7 Family) PCI Express Root Port - 27D6
[0000DC80 - 0000DC9F] Intel(R) 82583V Gigabit Network Connection
[0000EC80 - 0000ECBF] Intel(R) PRO/100 M Network Connection
[0000FFA0 - 0000FFAF] Intel(R) 82801G (ICH7 Family) Ultra ATA Storage Controllers - 27DF

3.5 Interrupt Controller (With CEB94000 under WinXP)


Interrupt request (IRQ)
(ISA) 0 System timer
(ISA) 1 Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
(ISA) 3 Communications Port (COM2)
(ISA) 4 Communications Port (COM1)
(ISA) 8 System CMOS/real time clock
(ISA) 9 Microsoft ACPI-Compliant System
(ISA) 12 Microsoft PS/2 Mouse
(ISA) 13 Numeric data processor
(ISA) 14 Primary IDE Channel
(PCI) 11 Intel(R) 82801G (ICH7 Family) SMBus Controller - 27DA
(PCI) 16 Intel(R) 82801G (ICH7 Family) PCI Express Root Port - 27D0
(PCI) 16 Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27CB
(PCI) 16 Microsoft UAA Bus Driver for High Definition Audio
(PCI) 16 Mobile Intel(R) 945 Express Chipset Family
(PCI) 18 Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27CA
(PCI) 19 Intel(R) 82583V Gigabit Network Connection
(PCI) 19 Intel(R) 82801G (ICH7 Family) PCI Express Root Port - 27D6
(PCI) 19 Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27C9
(PCI) 19 Intel(R) 82801GBM/GHM (ICH7-M Family) Serial ATA Storage Controller - 27C4
(PCI) 23 Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27C8
(PCI) 23 Intel(R) 82801G (ICH7 Family) USB2 Enhanced Host Controller - 27CC
(PCI) 23 Intel(R) PRO/100 M Network Connection

CHAPTER 4

AMI BIOS UTILITY

The BIOS of CEM831 is porting as legacy-free which is default to be without LPC I/O, the another alternative is with Winbond Super I/O W83627HG. If the Baseboard designer use a different Super I/O chip, the BIOS needs to be customized. The AMI BIOS provides users with a built-in Setup program to modify basic system configuration. All configured parameters are stored in a battery-backed-up RAM (CMOS RAM) to save the Setup information whenever the power is turned off.

4.1 Starting

To enter the setup screens, follow the steps below:

1. Turn on the computer and press the <Del> key immediately.
2. After you press the <Delete> key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as the Chipset and Power menus.

4.2 Navigation Keys

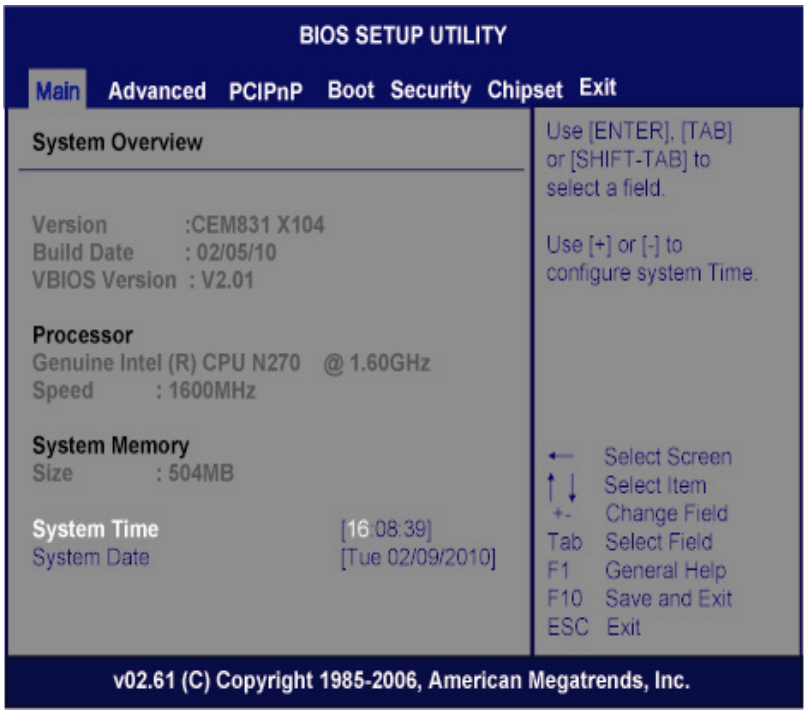
The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process.
These keys include <F1>, <F10>, <Enter>, <ESC>, <Arrow> keys, and so on.

Note *Some of navigation keys differ from one screen to another.*

← Left/Right	The Left <Arrow> keys allow you to select a setup screen.
↑↓ Up/Down	The Up and Down <Arrow> keys allow you to select a setup screen or sub-screen.
+– Plus/Minus	The Plus and Minus <Arrow> keys allow you to change the field value of a particular setup item.
Tab	The <Tab> key allows you to select setup fields.
F1	The <F1> key allows you to display the General Help screen.
F10	The <F10> key allows you to save any changes you have made and exit Setup. Press the <F10> key to save your changes.
Esc	The <Esc> key allows you to discard any changes you have made and exit the Setup. Press the <Esc> key to exit the setup without saving your changes.
Enter	The <Enter> key allows you to display or change the setup option listed for a particular setup item. The <Enter> key can also allow you to display the setup sub- screens.

4.3 Main Menu

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



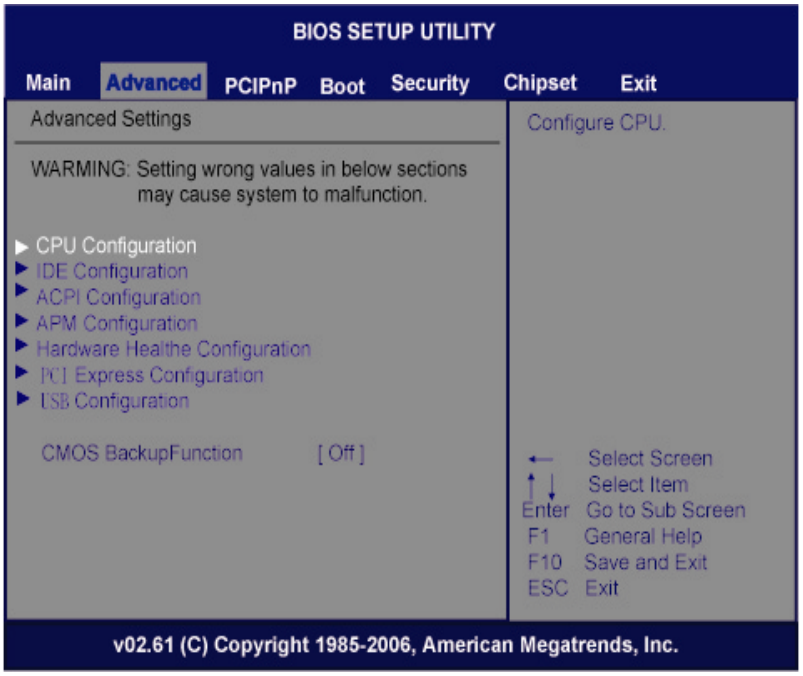
- **System Time/Date**
  Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

4.4 Advanced Menu

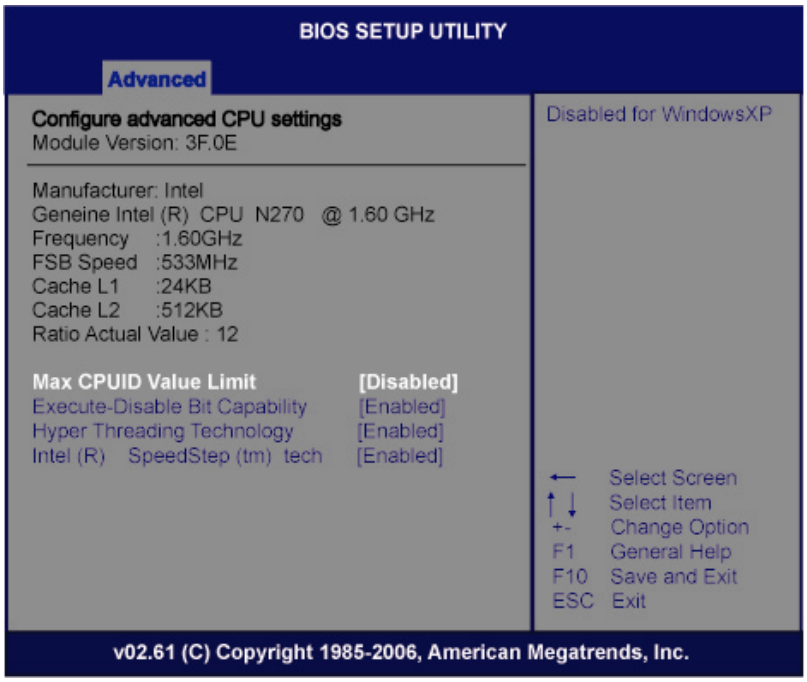
The Advanced menu allows users to set configuration of the CPU and other system devices. You can select any of the items in the left frame of the screen to go to the sub menus:

- CPU Configuration
- IDE Configuration
- ACPI Configuration
- APM Configuration
- Hardware Health CPU Configuration
- PCI Express Configuration
- USB Configuration

For items marked with "►", please press <Enter> for more options.



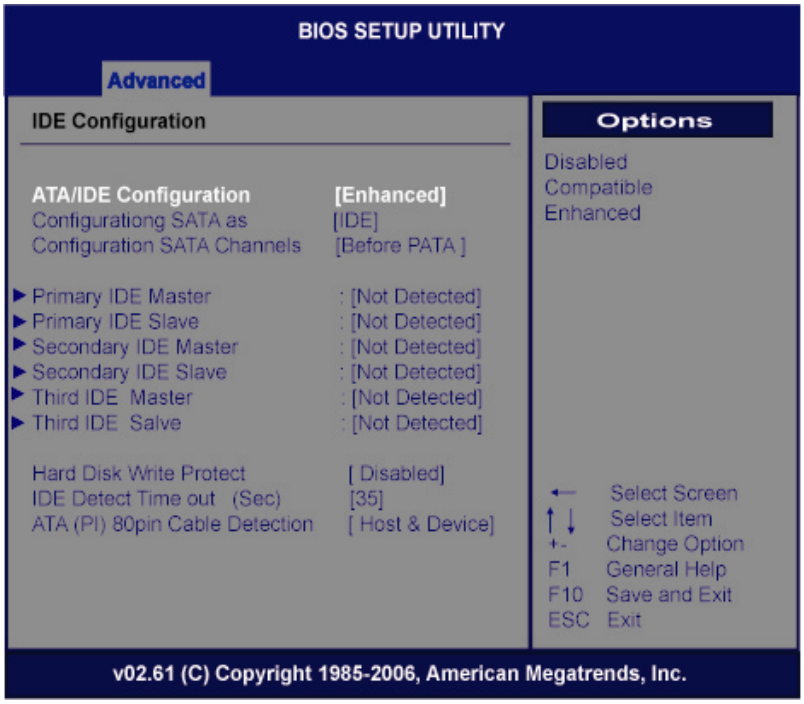
- **CPU Configuration**
  This screen shows the CPU Configuration, and you can change the value of the selected option.



  - Max CPUID Value Limit
    You can enable this item to let legacy operating systems boot even without support for CPUs with extended CPU ID functions.
  - Execute-Disable Bit Capability
    This item helps you enable or disable the No-Execution Page Protection Technology.
  - Hyper Threading Technology
    Use this item to enable or disable Hyper-Threading Technology, which makes a single physical processor perform multi-tasking function as two logical ones.

- Intel (R) Speed Step (tm) tech
  This item helps you enable or disable the Intel Speed Step Technology.
- Intel (R) C-STATE tech
  Use this item to enable or disable the C-State technology.
- Enhanced C-States
  This item allows you to enable or disable any available enhanced C-states (C1E, C2E, C3E, C4E and Hard C4E).

- **IDE Configuration**
  You can use this screen to select options for the IDE Configuration, and change the value of the selected option. A description of the selected item appears on the right side of the screen. For items marked with "▶", please press <Enter> for more options.


BIOS SETUP UTILITY
Advanced
IDE Configuration
ATA/IDE Configuration [Enhanced]
Configurationg SATA as [IDE]
Configuration SATA Channels [Before PATA]
▶ Primary IDE Master : [Not Detected]
▶ Primary IDE Slave : [Not Detected]
▶ Secondary IDE Master : [Not Detected]
▶ Secondary IDE Slave : [Not Detected]
▶ Third IDE Master : [Not Detected]
▶ Third IDE Salve : [Not Detected]
Hard Disk Write Protect [Disabled]
IDE Detect Time out (Sec) [35]
ATA (PI) 80pin Cable Detection [Host & Device]
Options
Disabled
Compatible
Enhanced
Select Screen
Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
v02.61 (C) Copyright 1985-2006, American Megatrends, Inc.

- **ATA/IDE Configuration**
  Use this item to specify the integrated IDE controller. There are three options for your selection: *Disabled*, *Compatible* and *Enhanced*.

- **Legacy IDE Channels**
  When the ATA/IDE Configuration is set to *Compatible*, this item will be displayed.

- **Primary/Secondary/Third IDE Master/Slave**
  Select one of the hard disk drives to configure IDE devices installed in the system by pressing <Enter> for more options.

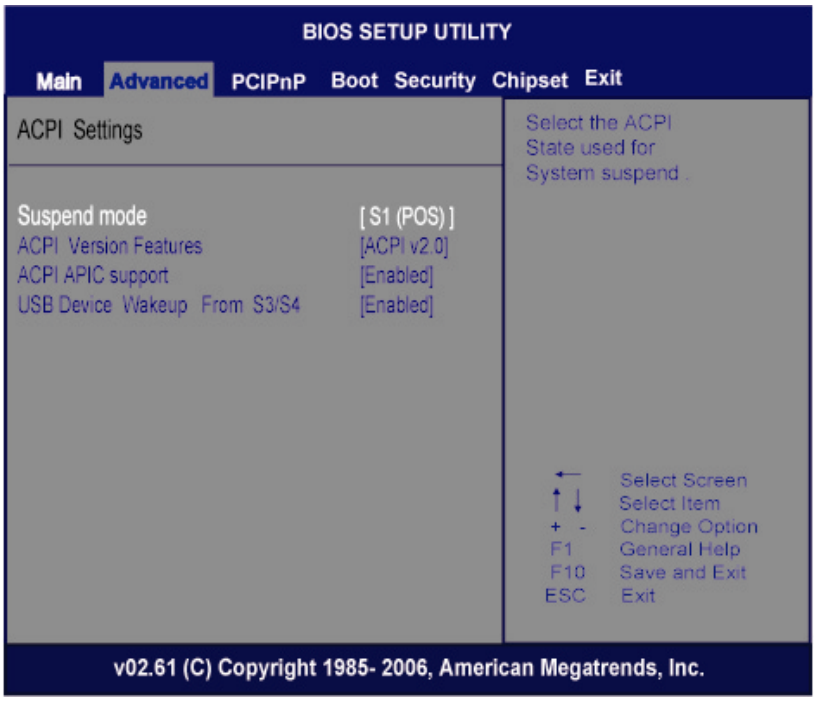
- **Primary/Secondary IDE Master/Slave**
  Select one of the hard disk drives to configure IDE devices installed in the system by pressing <Enter> for more options.

- **Third IDE Master**
  Select one of the hard disk drives to configure IDE devices installed in the system by pressing <Enter> for more options.

- **Hard Disk Write Protect**
  Set this option to protect the hard disk drive from being overwritten. The default setting is *Disabled*.

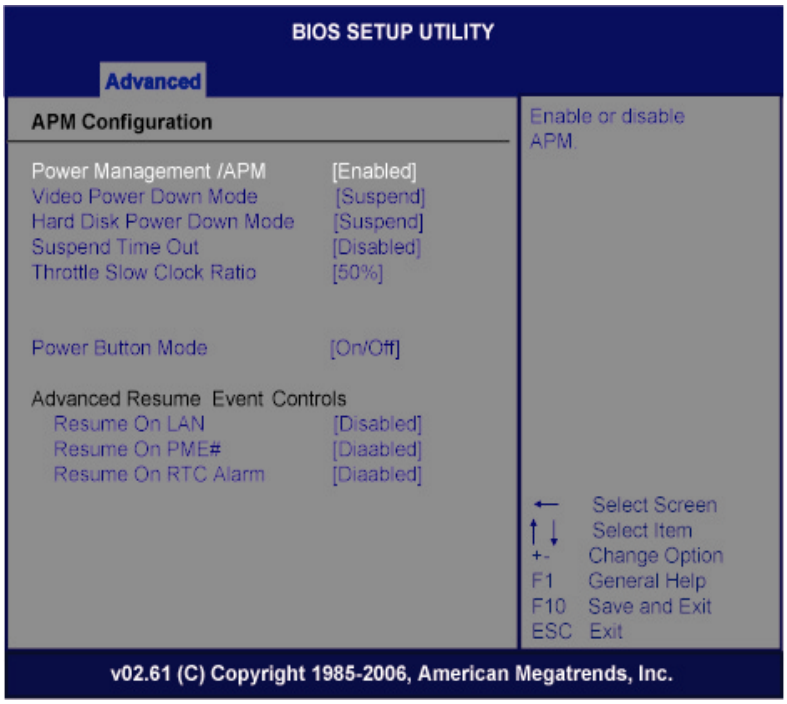
- **IDE Detect Time Out (Sec)**
  Set this option to stop the AMIBIOS from searching for IDE devices within the specified number of seconds. Basically, this allows you to fine-tune the settings to allow for faster boot times. Adjust this setting until a suitable timing that can detect all IDE disk drives attached is found.

- **ACPI Configuration**
  You can use this screen to select options for the ACPI Configuration, and change the value of the selected option. A description of the selected item appears on the right side of the screen.


BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Exit
ACPI Settings
Suspend mode [S1 (POS)]
ACPI Version Features [ACPI v2.0]
ACPI APIC support [Enabled]
USB Device Wakeup From S3/S4 [Enabled]
Select the ACPI State used for System suspend .
Select Screen
Select Item
+ - Change Option
F1 General Help
F10 Save and Exit
ESC Exit
v02.61 (C) Copyright 1985- 2006, American Megatrends, Inc.

  - **Suspend Mode**
    This item selects the Advanced Configuration and Power Interface (ACPI) state for system suspend.
  - **ACPI Version Features**
    Use this item to set the system to be complaint with the ACPI 2.0 specification.
  - **ACPI APIC support**
    This item allows you to enable or disable the Advanced Configuration and Power Interface (ACPI) support in the Application-Specific Integrated Circuit (APIC). Enabling this item makes the RSDT pointer list include the ACPI APIC table pointer.

- **APM Configuration**
  You can use this screen to select options for the APM Configuration, and change the value of the selected option. A description of the selected item appears on the right side of the screen.



  - **Power Management/APM**
    Set this item to allow Power Management/APM support. The default setting is *Enabled*.

Disabled	Set this item to prevent the chipset power management and APM (Advanced Power Management) features.
Enabled	Set this item to allow the chipset power management and APM (Advanced Power Management) features. This is the default setting.

- **Power Button Mode**

  This option specifies how the externally mounted power button on the front of the computer chassis is used. The default setting is *On/Off*.

On/Off	Pushing the power button turns the computer on or off. This is the default setting. This is the default setting.
Suspend	Pushing the power button places the computer in Suspend mode or Full On power mode.

- **Video Power Down Mode**

  This option specifies the Power State that the video subsystem enters when the BIOS places it in a power saving state after the specified period of display inactivity has expired. The default setting is *Suspend*.

Disabled	This setting prevents the BIOS from initiating any power saving modes concerned with the video display or monitor.
Standby	This option places the monitor into standby mode after the specified period of display inactivity has expired. This means the monitor is not off. The screen will appear blacked out. The standards do not cite specific power ratings because they vary from monitor to monitor.
Suspend	This option places the monitor into suspend mode after the specified period of display inactivity has expired. This means the monitor is not off. The screen will appear blacked out. The standards do not cite specific power ratings because they vary from monitor to monitor, but this setting use less power than Standby mode. This is the default setting.

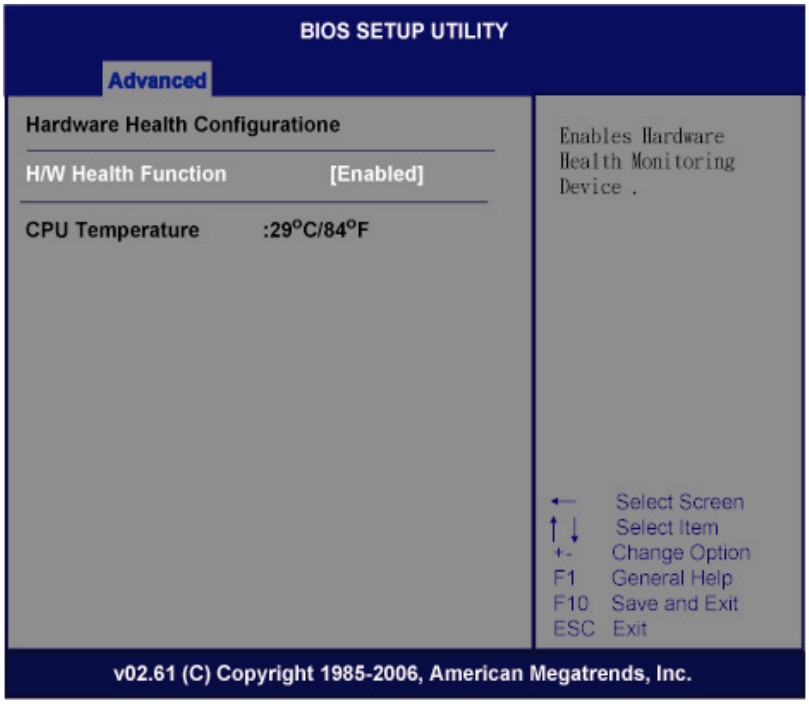
- **Hard Disk Drive Power Down Mode**
  This option specifies the power conserving state that the hard disk drive enters after the specified period of hard drive inactivity has expired. The default setting is *Suspend*.

Disabled	This setting prevents hard disk drive power down mode.
Standby	This option stops the hard disk drives from spinning during a system standby.
Suspend	This option cuts the power to the hard disk drives during a system suspend. This is the default setting.

- **Resume On PME#**
  This item enables or disables the function of Resume On PME# (Power Management Event). Enabling this item allows the system to resume from standby mode.

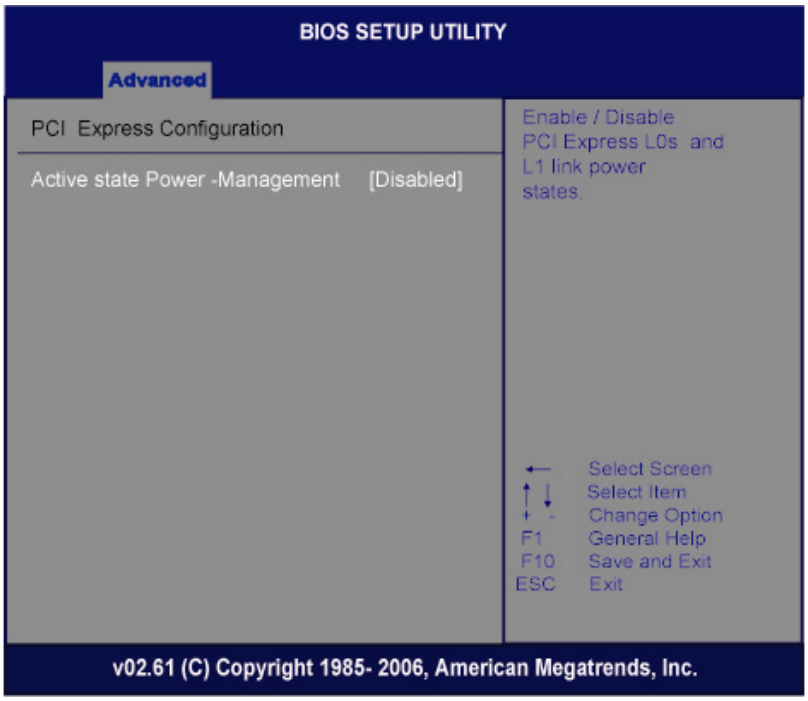
- **Resume On RTC Alarm**
  You can set "Resume On RTC Alarm" item to enabled and key in Data/time to power on system.

- **Hardware Health CPU Configuration**
  This screen shows the Hardware Health CPU Configuration, and a description of the selected item appears on the right side of the screen.



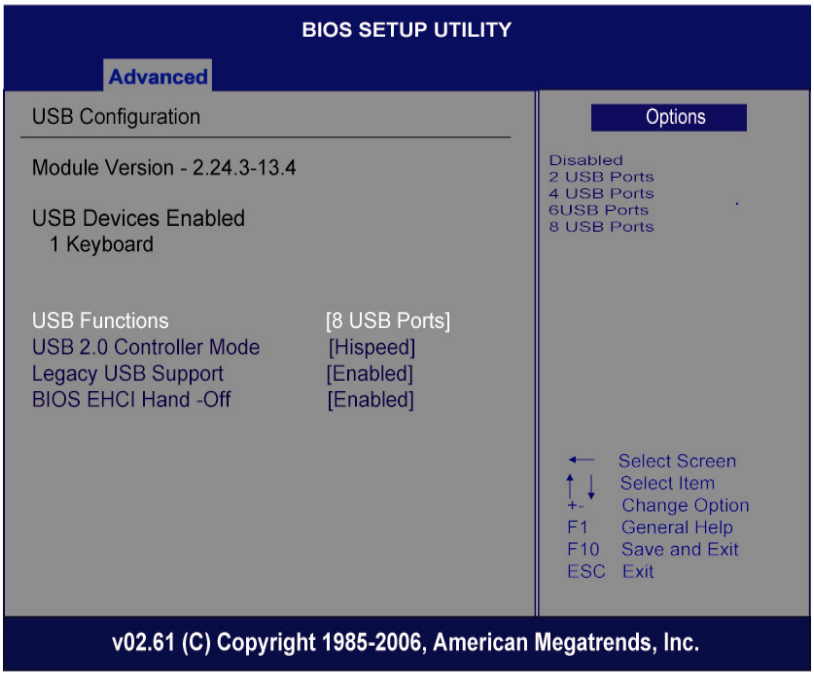
  - **H/W Health Function**
    If you computer contains a monitoring system, it will show PC health status during POST stage. There are these options for your selection: *Enabled* and *Disabled*.
  - **Hardware Health Event Monitoring**
    The Hardware Health Event Monitoring displays the temperature of CPU and System, Fan Speed, Vcore, etc.
  - **System Temperature/CPU Temperature/Fan2 Speed**
    These items display the temperature of CPU and System, Fan Speed, Vcore, etc.

- **PCI Express Configuration**
  This screen shows the PCI Express Configuration, and you can change its value. A description of the selected item appears on the right side of the screen.



  - **Active State Power-Management**
    Use this item to enable or disable the function of Active State Power-Management to provide you with lower power consumption. The default setting is *Disabled*.

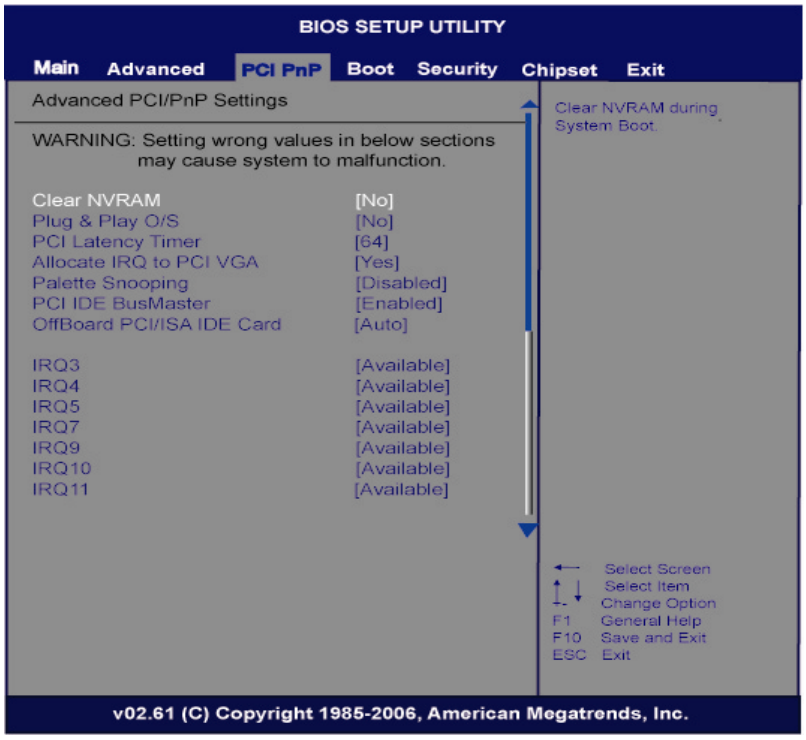
- **USB Configuration**
  You can use this screen to select options for the USB Configuration, and change the value of the selected option. A description of the selected item appears on the right side of the screen.



  - **USB 2.0 Controller Mode**
    Use this item to configure the USB 2.0 controller. The default setting is *HiSpeed*.
  - **Legacy USB Support**
    Use this item to enable or disable support for USB device on legacy operating system. The default setting is *Enabled*.
  - **BIOS EHCI Hand-Off**
    Enabling this item provide the support for operating systems without an EHCI hand-off feature. The default setting is *Enabled*.

4.5 PCI PnP Menu

The PCI PnP menu allows users to change the advanced settings for PCI/PnP devices.



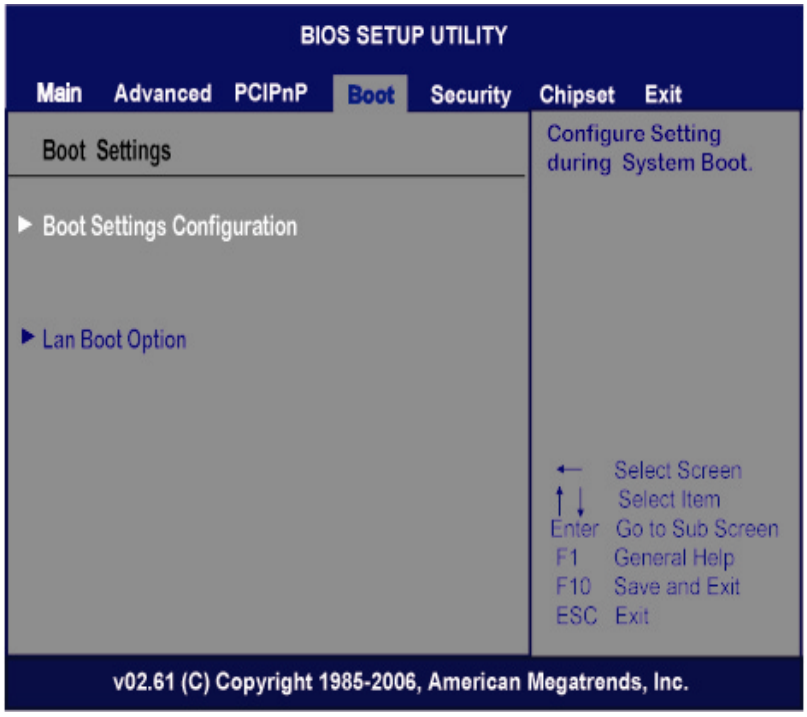
- **Plug & Play O/S**
  When the setting is No, Use this item to configure all the devices in the system. When the setting is Yes and if you install a Plug and Play operating system, the operating system configures the Plug and Play devices not required for boot. The default setting is *No*.

4.6 Boot Menu

The Boot menu allows users to change boot options of the system. You can select any of the items in the left frame of the screen to go to the sub menus:

- Boot Settings Configuration
- Boot Device Priority
- Hard Disk Drives
- INTEL 82574 LAN Boot ROM

For items marked with "►", please press <Enter> for more options.


BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Exit
Boot Settings
Configure Setting during System Boot.
► Boot Settings Configuration
► Lan Boot Option
← Select Screen
↑↓ Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
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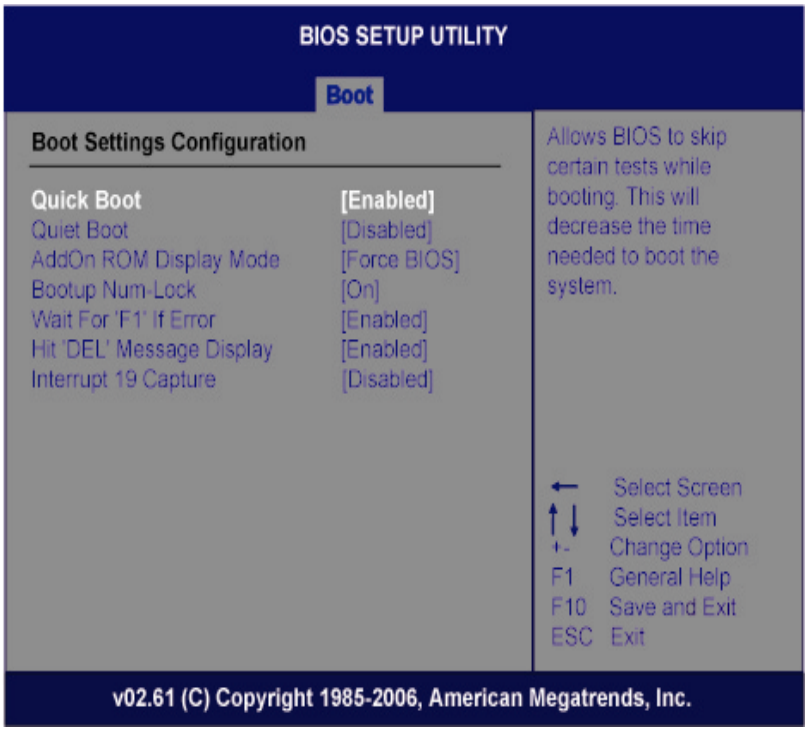
- **Boot Settings Configuration**


BIOS SETUP UTILITY
Boot
Boot Settings Configuration
Quick Boot [Enabled]
Quiet Boot [Disabled]
AddOn ROM Display Mode [Force BIOS]
Bootup Num-Lock [On]
Wait For 'F1' If Error [Enabled]
Hit 'DEL' Message Display [Enabled]
Interrupt 19 Capture [Disabled]
Allows BIOS to skip certain tests while booting. This will decrease the time needed to boot the system.
Select Screen
Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
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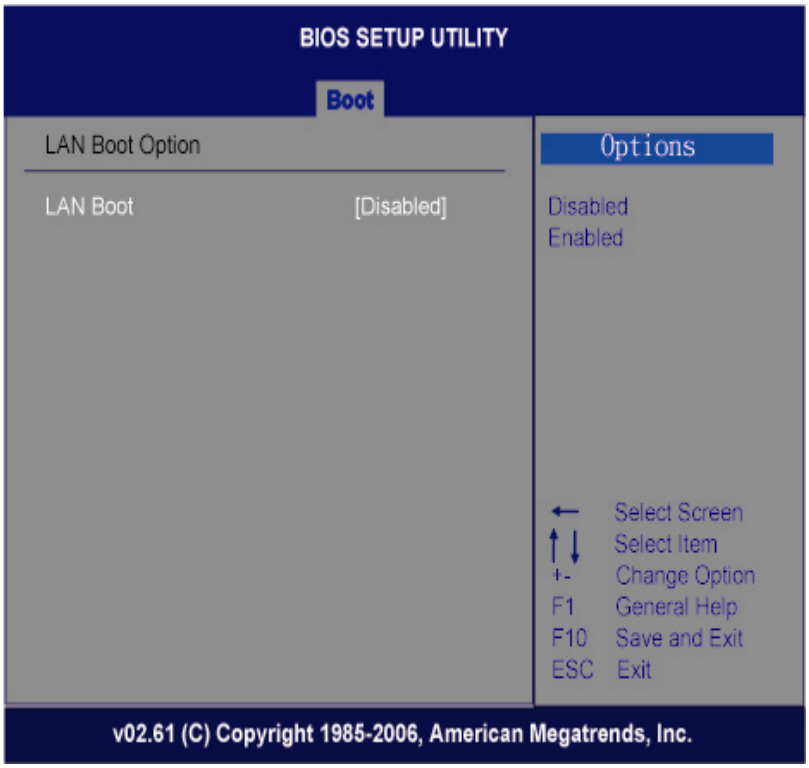
  - **Quick Boot**
    Enabling this item lets the BIOS skip some power on self tests (POST). The default setting is *Enabled*.
  - **Quiet Boot**

Disabled	Set this item to allow the computer system to display the POST messages.
Enabled	Set this item to allow the computer system to display the OEM logo. This is the default setting.

  - **AddOn ROM Display Mode**
    This item selects the display mode for option ROM. The default setting is *Force BIOS*.
  - **Boot Num-Lock**
    Use this item to select the power-on state for the NumLock. The default setting is *On*.

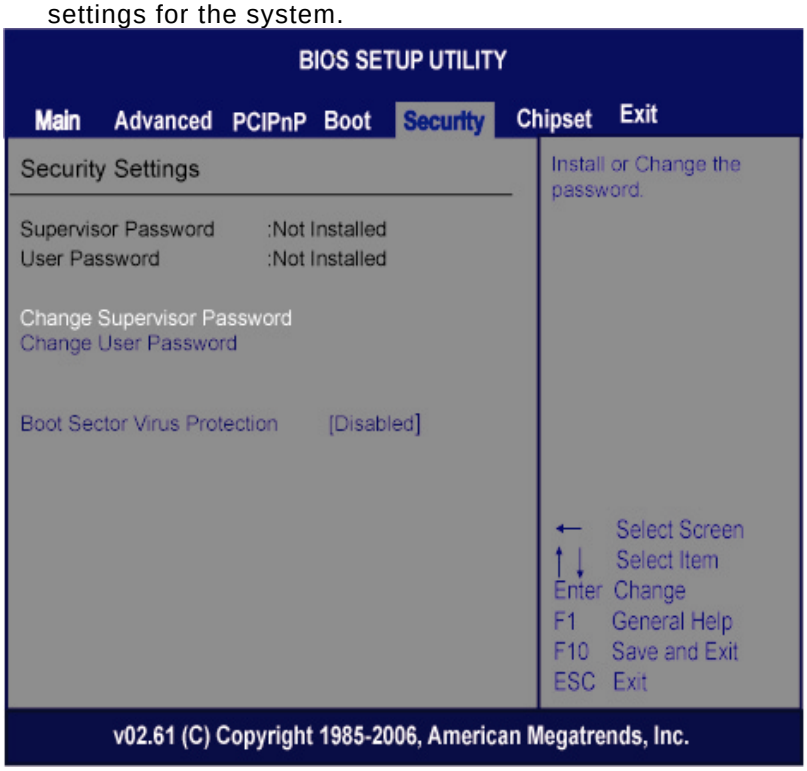
- **Wait For 'F1' Of Error**
  If this item is enabled, the system waits for the F1 key to be pressed when error occurs. The default setting is *Enabled*.
- **Hit 'DEL' Message Display**
  If this item is enabled, the system displays the message "Press DEL to run Setup" during POST. The default setting is *Enabled*.
- **Interrupt 19 Capture**
  If this item is enabled, this function makes the option ROMs to trap Interrupt 19. The default setting is *Disabled*.

- **LAN Boot Option**



4.7 Security Menu

The Security menu allows users to change the security settings for the system.



- **Supervisor Password**
  This item indicates whether a supervisor password has been set. If the password has been installed, Installed displays. If not, Not Installed displays.

- **User Password**
  This item indicates whether a user password has been set. If the password has been installed, Installed displays. If not, Not Installed displays.

- **Change Supervisor Password**
  Select this option and press <Enter> to access the sub menu. You can use the sub menu to change the supervisor password.
- **Change User Password**
  Select this option and press <Enter> to access the sub menu. You can use the sub menu to change the user password.
- **Boot Sector Virus Protection**
  This option is near the bottom of the Security Setup screen. The default setting is *disabled*.

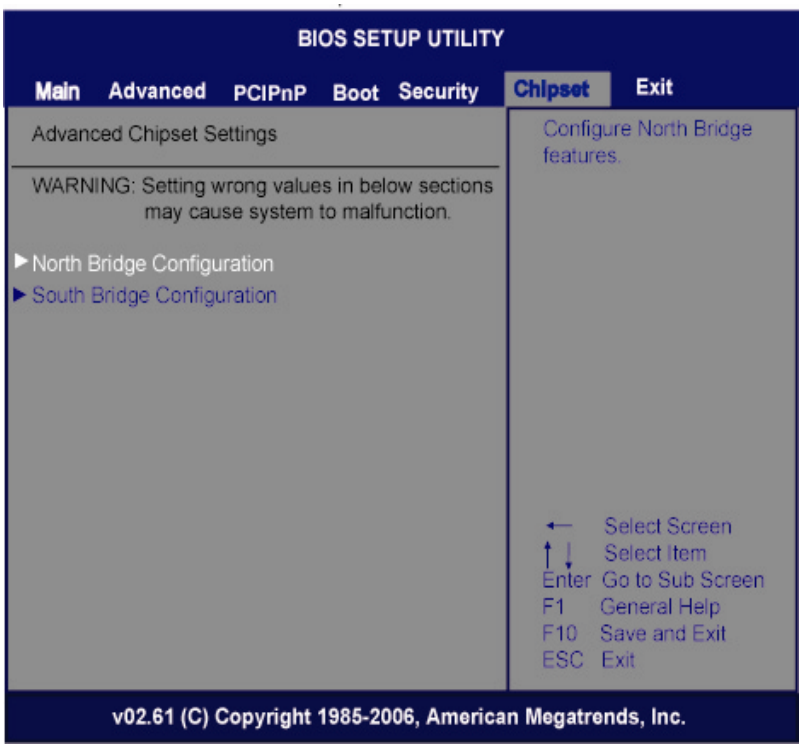
Disabled	Set this item to prevent the Boot Sector Virus Protection. This is the default setting.
Enabled	Select Enabled to enable boot sector protection. It displays a warning when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive. If enabled, the following appears when a write is attempted to the boot sector. You may have to type N several times to prevent the boot sector write. Boot Sector Write! Possible VIRUS: Continue (Y/N)? _ The following appears after any attempt to format any cylinder, head, or sector of any hard disk drive via the BIOS INT 13 Hard disk drive Service: Format!!! Possible VIRUS: Continue (Y/N)?

4.8 Chipset Menu

The Chipset menu allows users to change the advanced chipset settings. You can select any of the items in the left frame of the screen to go to the sub menus:

- North Bridge Configuration
- South Bridge Configuration

For items marked with "►", please press <Enter> for more options.


BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Exit
Advanced Chipset Settings
WARNING: Setting wrong values in below sections may cause system to malfunction.
North Bridge Configuration
South Bridge Configuration
Configure North Bridge features.
Select Screen
Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
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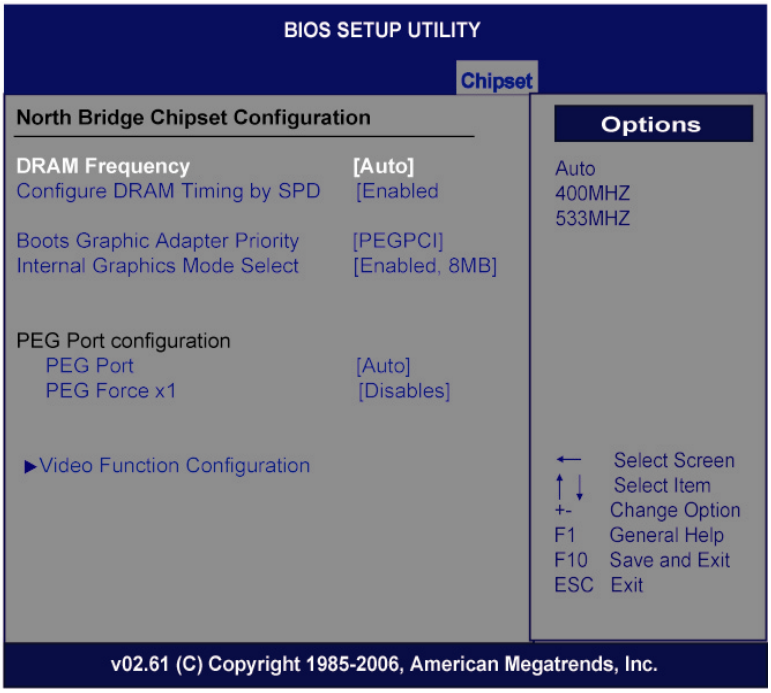
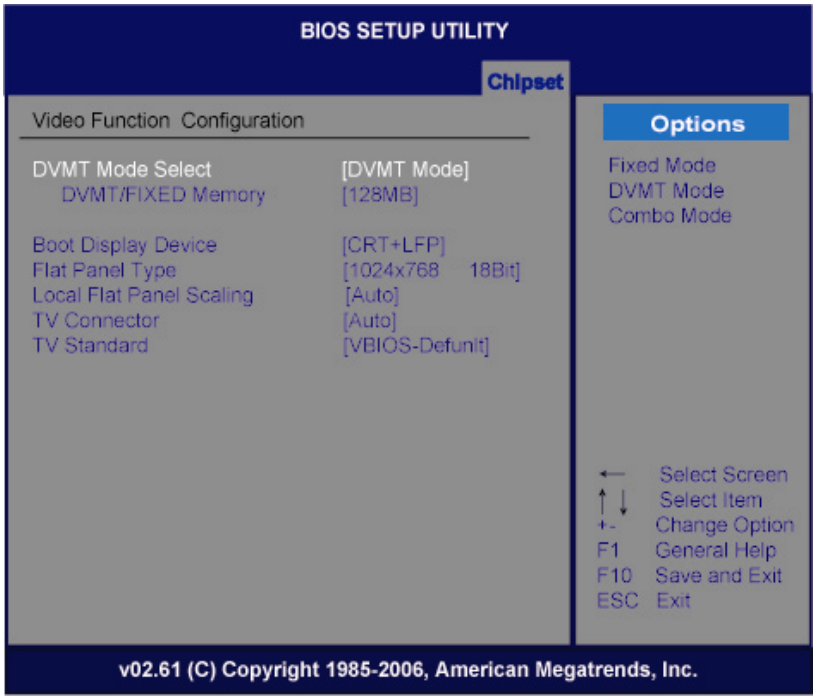
- **North Bridge Configuration**

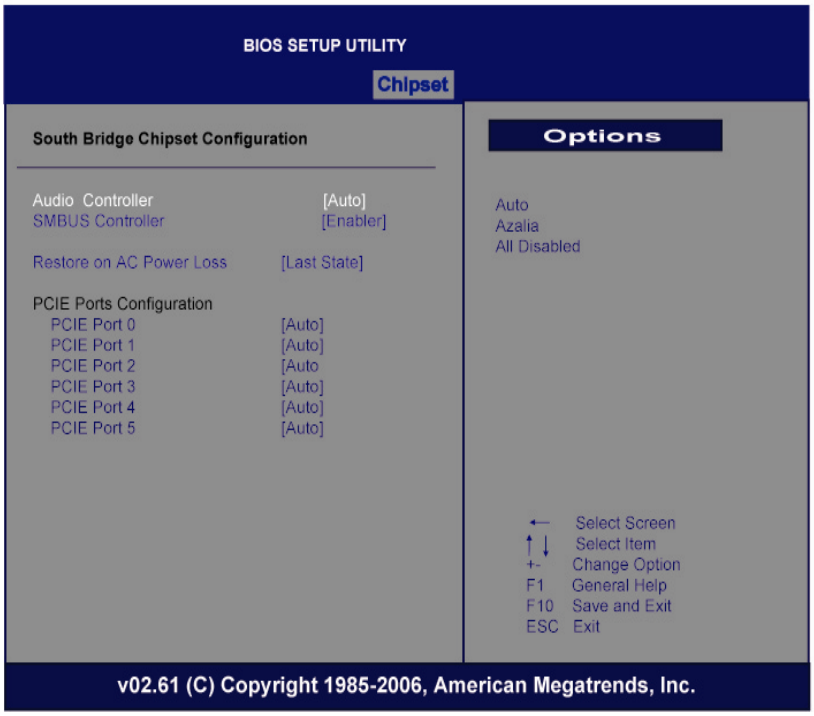


  - **Boot Graphic Adapter Priority**
    This item allows you to select the graphics controller as the primary boot device.
  - **Internal Graphics Mode Select**
    This item allows you to select the amount of system memory used by the internal graphics device.
  - **PEG Port Configuration/PEG Port**
    This item is a toggle to enable or disable the PCI Express port. Here are the options for your selection, *Auto* and *Disabled*.
  - **Video Function Configuration**
    Press <Enter> for the sub-menu for setting up video function.

- **Video Function Configuration**



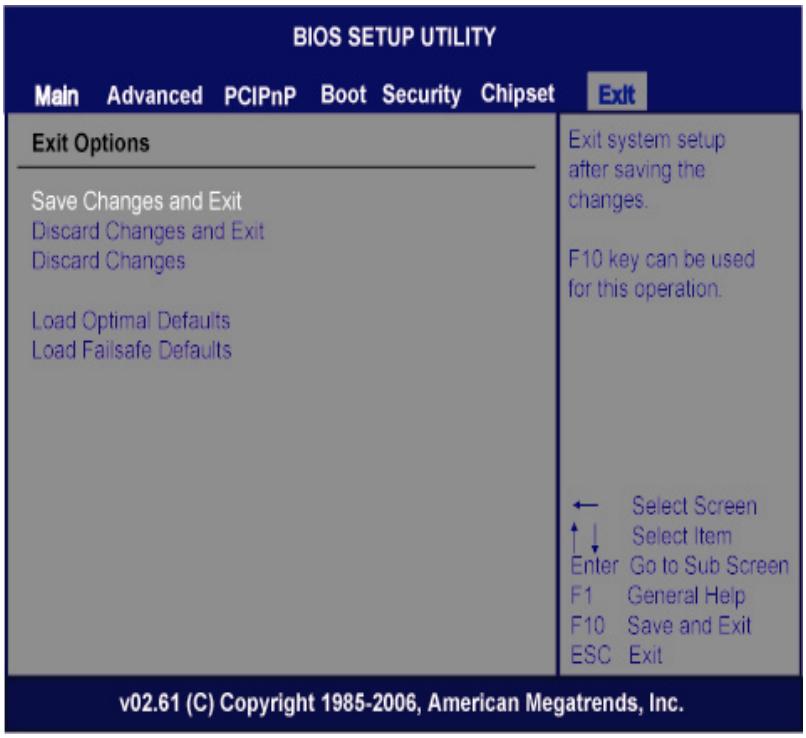
- **South Bridge Configuration**



  - **PCIE Port Configuration**
    This item allows you to set or disable the PCI Express Ports.

4.9 Exit Menu

The Exit menu allows users to load your system configuration with optimal or failsafe default values.


BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Exit
Exit Options
Save Changes and Exit
Discard Changes and Exit
Discard Changes
Load Optimal Defaults
Load Failsafe Defaults
Exit system setup after saving the changes.
F10 key can be used for this operation.
← Select Screen
↑ ↓ Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
v02.61 (C) Copyright 1985-2006, American Megatrends, Inc.

- **Save Changes and Exit**

  When you have completed the system configuration changes, select this option to leave Setup and reboot the computer so the new system configuration parameters can take effect. Select *Save Changes and Exit* from the Exit menu and press <Enter>. Select Ok to save changes and exit.

- **Discard Changes and Exit**
  Select this option to quit Setup without making any permanent changes to the system configuration. Select *Discard Changes and Exit* from the Exit menu and press <Enter>. Select Ok to discard changes and exit.

- **Load Optimal Defaults**
  It automatically sets all Setup options to a complete set of default settings when you select this option. The Optimal settings are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Optimal Setup options if your computer is experiencing system configuration problems. Select Load Optimal Defaults from the Exit menu and press <Enter>.

- **Load Fail-Safe Defaults**
  It automatically sets all Setup options to a complete set of default settings when you select this option. The Fail-Safe settings are designed for maximum system stability, but not maximum performance. Select the Fail-Safe Setup options if your computer is experiencing system configuration problems. Select Load Fail-Safe Defaults from the Exit menu and press <Enter>. Select Ok to load Fail-Safe defaults.

APPENDIX A

WATCHDOG TIMER

Watchdog Timer Setting (From CEB94000 Super I/O W83627HG)

After the system stops working for a while, it can be auto-reset by the Watchdog Timer. The integrated Watchdog Timer can be set up in the system reset mode by program.

Using the Watchdog Function

Start

↓

Un-Lock WDT:

O 2E 87 ; Un-lock super I/O
O 2E 87 ; Un-lock super I/O

↓

Select Logic device:

O 2E 07
O 2F 08

↓

Activate WDT:

O 2E 30
O 2F 01

↓

Set Second or Minute :

O 2E F5
O 2F N N=00 or 08(See below table)

↓

Set base timer :

O 2E F6
O 2F M=00,01,02,…FF(Hex) ,Value=0 to 255

↓

WDT counting re-set timer :

O 2E F6
O 2F M ; M=00,01,02,…FF(See below table)

; IF to disable WDT:

O 2E 30
O 2F 00 ; Can be disable at any time

- Timeout Value Range
  - 1 to 255
  - Minute / Second
- Program Example

  Watchdog Timer can be set to system reset after 5-second timeout.

O 2E, 87	
O 2E, 87	
O 2E. 07	
O 2F, 08	Logical Device 8
O 2E, 30	Activate
O 2F, 01	
O 2E, F5	
O 2F, N	Set Minute or Second N=08 (Min),00(Sec)
O 2E, F6	
O 2F, M	Set Value M = 00 ~ FF

APPENDIX B

GPIO & WATCHDOG TIMER PROGRAMMING SOURCE CODE (FROM CEM831 FINTEK F75111R)

Programming Source Code

```
/*---------------- INCLUDE FILE ----------------------*/
#include <stdio.h>
#include <conio.h>
#include <bios.h>

#define UCHAR   unsigned char
#define UINT    unsigned int
#define SMIOBASE       0x400
/*****************
      SMIOBASE can get from PCI device Bus-0,Device-31,
Function-3
      Register 20h~23h, the value is the IO base address.
******************/
#define SM_REG         (SMIOBASE+3)
#define SM_ADDR        (SMIOBASE+4)
#define SM_DATA        (SMIOBASE+5)
#define SM_CMD         (SMIOBASE+2)
#define SM_STATUS      (SMIOBASE+0)
#define SM_byteAccess   0x48
#define Device_Addr     0x6E  //depend on hardwire designed
UCHAR _read_smbus(UCHAR ,UCHAR);
void _write_smbus(UCHAR,UCHAR, UCHAR);
#define F75111_CHIPID   0x0003
#define F75111_VENDORID 0x3419
#define WDTOUT10_CntlReg1      0x34
#define WDTOUT10_2S_bit        0x04    //bit 2
#define WDTOUT10_OINV_bit      0x02    //bit 1
#define WDTOUT10_Status_bit    0x01    //bit 0 , write 1 for clear
status
#define WDTOUT10_CntlReg2      0x35
#define WDTOUT10_Enable_bit    0x80    //bit 7
#define WDTOUT10_PTIME         0x7f    //bit 0~6

/* ----------------- MAIN PROGRAM -----------------*/
```

```
main()
{
UCHAR   xch,xch2;
UINT    chipid=0, vendorid=0;
      //Check the Chip ID information
      xch=_read_smbus(Device_Addr,0x5a);      //Chip ID 1
      xch2=_read_smbus(Device_Addr,0x5b);     //Chip ID 2
      chipid=((UINT)xch2 << 8) + (UINT)xch;
      xch=_read_smbus(Device_Addr,0x5d);      //Vendor ID 1
      xch2=_read_smbus(Device_Addr,0x5E);     //Vendor ID 2
      vendorid=((UINT)xch2 << 8) + (UINT)xch;
      if (F75111_CHIPID != chipid || F75111_VENDORID != vendorid )
        { printf("!!! Not found F75111 chip !!!\n");
          exit(-1);
        }
      printf("=== Found F75111 chip ===\n");
      printf("=== GPIO Output Test ===\n");

      //set GPIO3x  direction
      printf("Set F75111 GPIO3x pin is output direction\n");
      _write_smbus(Device_Addr,0x40,0x0f);  //GPIO3x Output
direction

      //set GPIO3x output level or plus
      printf("Set F75111 GPIO3x pin is output Level\n");
      _write_smbus(Device_Addr,0x43,0);  //GPIO3x Level control

      //write GPIO3x data
      printf("Write GPIO3x data is 0x0A\n");
      printf("GPO0=0, GPO1=1, GPO2=0, GPO3=1\n");
      _write_smbus(Device_Addr,0x41,0x0a);
      printf("Please check the GPO level and hit any key to
continue\n");
      getch();

      //write GPIO3x data
      printf("Write GPIO3x data is 0x05\n");
      printf("GPO0=1, GPO1=0, GPO2=1, GPO3=0\n");
      _write_smbus(Device_Addr,0x41,0x05);
      printf("Please check the GPO level and hit any key to
continue\n");
      getch();
```

```
      //set GPIO10,11,12 used
      printf("=== GPIO Input Test ===\n");
      printf("Set F75111 GPIO1x is used GPIO function\n");
      xch=_read_smbus(Device_Addr,0x03);
      xch &= 0xE0 ;
      _write_smbus(Device_Addr,0x03,xch);  //set Pin GPIO10/11/12
used
      _write_smbus(Device_Addr,0x04,0);    //set Pin GPIO1x used

      printf("Set F75111 GPIO10,11,12,13 is input function\n");
      _write_smbus(Device_Addr,0x10,0x00);  //set GPIO1x input
direction

      printf("Set F75111 GPIO10,11,12,13 is Level mode\n");
      _write_smbus(Device_Addr,0x13,0x00);  //set GPIO1x Level
Control

      xch=_read_smbus(Device_Addr,0x12);    //read GPIO1x Status
      printf("Read the GPI0,1,2,3 input data is %02X\n",xch);
      printf("Please Change the GPIx input and hit any key to
continue\n");
      getch();
      xch=_read_smbus(Device_Addr,0x12);    //read GPIO1x Status
      printf("Read the GPI0,1,2,3 input data is %02X\n",xch);
      printf("Please Change the GPIx input and hit any key to
continue\n");
      getch();
      xch=_read_smbus(Device_Addr,0x12);    //read GPIO1x Status
      printf("Read the GPI0,1,2,3 input data is %02X\n",xch);
      /*****************************************/
      printf("===== WatchDogTimer Test =====\n");
      printf("Set WDTOUT10 pin used\n");
      _write_smbus(Device_Addr,0x01,0x20);  //Pin1 config

      printf("Set WDTOUT10 output 100ms plus, normal level\n");
      _write_smbus(Device_Addr,WDTOUT10_CntlReg1,0);
//WDT10 control

      printf("Set WDTOUT10 Time 10 seconds and enable WDT\n");
      _write_smbus(Device_Addr,WDTOUT10_CntlReg2,0x8A);
//WDT10 control
```

```
 printf("Please hit any key in period of 10 seconds\n");
      getch();
      _write_smbus(Device_Addr,WDTOUT10_CntlReg2,0x8A);
//WDT10 control
      printf("The sytsem will reset when the 10 seconds times
out\n");
}
void _write_smbus(UCHAR xAddr,UCHAR xReg, UCHAR xData)
{
      while (1)
      { if (_check_smbus_busy()==0) break;
      }
      outp(SM_REG, xReg);
      xdelay();           //because the CPU too fast,delay for IO
      outp(SM_ADDR, xAddr);
      xdelay();           //because the CPU too fast,delay for IO
      outp(SM_DATA, xData);
      xdelay();           //because the CPU too fast,delay for IO
      outp(SM_CMD, SM_byteAccess);
      xdelay();           //because the CPU too fast,delay for IO
      outp(SM_STATUS, 02);    //clear interrupt status
}
UCHAR _read_smbus(UCHAR xAddr,UCHAR xReg)
{
UCHAR   xch,xch2;
      while (1)
      { if (_check_smbus_busy()==0) break;
      }
      outp(SM_REG, xReg);
      xdelay();           //because the CPU too fast,delay for IO
      outp(SM_ADDR, xAddr+1);
      xdelay();           //because the CPU too fast,delay for IO
      outp(SM_CMD, SM_byteAccess);
      xdelay();           //because the CPU too fast,delay for IO
      while (1)
      { if (_check_smbus_busy()==0) break;
      }
      xch=inp(SM_DATA);
      xdelay();           //because the CPU too fast,delay for IO
      outp(SM_STATUS, 2);    //clear interrupt status
      return xch;
}
_check_smbus_busy(void)
{
UCHAR   xch;
      xch=inp(SM_STATUS);
```

```
        if (xch & 0x02 ) outp(SM_STATUS, 2);    //clear interrupt
status
        if ( xch & 0x02 ) return 1;
        if ( xch & 0x01 ) return 1;
        return 0;
}
xdelay()
{
int     xxi,xxj,xxk=0;
        for (xxi=0 ; xxi< 0x1000 ; xxi++) {
                for (xxj=0 ; xxj < 0x100 ; xxj++) {
                        xxk++;
                }
        }
}
```